IN THE SPECIFICATION:

Please amend paragraph **[0006]** as follows:

[0006] "Flip-chip" technology, as originating with controlled collapse chip connection (C-4) technology, is an example of an assembly and packaging technology that results in a semiconductor device being oriented substantially parallel to a carrier substrate, such as a circuit board. In flip-chip technology, the bond pads or contact pads of a semiconductor device are arranged in an array over a major surface of the semiconductor device. Flip-chip techniques are applicable to both bare and packaged semiconductor devices. A packaged flip-chip type semiconductor device, which typically has solder balls arranged in a so-called "ball grid array" (BGA) connection pattern, typically includes a semiconductor die and a carrier substrate, which is typically termed an ~~"interposer".~~ "interposer." The interposer may be positioned adjacent either the back side of the semiconductor die or the active (front) surface thereof.

Please amend paragraph **[0007]** as follows:

[0007] When the interposer is positioned adjacent the back side of the semiconductor die, the bond pads of the semiconductor die are typically electrically connected by way of wire bonds or other intermediate conductive elements to corresponding contact areas on a top side of the interposer. These contact areas communicate with corresponding bumped contact pads on the back side of the interposer. This type of flip-chip assembly is positioned adjacent a ~~higher-level~~ higher-level carrier substrate with the back side of the interposer facing the carrier substrate.

Please amend paragraph **[0027]** as follows:

[0027] In another method for assembling a semiconductor device package in accordance with teachings of the present invention, (a) first-level semiconductor devices are singulated and attached, flip-chip style, to the active surface of the second-level semiconductor devices, typically with a BGA, (b) the second-level semiconductor devices, carrying the ~~first-level~~ first-level semiconductor devices, are singulated and attached to the interposers in flip-chip style (active surface down), so that the first-level semiconductor devices are enclosed in the

interposer receptacles, and (c) the sheet or strip of packages is encapsulated and individual packages singulated from the sheet or strip.

Please amend paragraph **[0054]** as follows:

[0054] Referring to FIG. 1, a multichip semiconductor device package 10 according to the present invention is illustrated. As shown, FIG. 1 is an external view of the package 10 and is representative of a large number of possible device configurations exemplified in the figures following FIG. 1. Package 10 is illustrated as having an upper surface 12, a lower surface 14, and peripheral edges 16. Outer connectors 18, shown here as solder balls in a ball grid array (BGA) connection pattern, are depicted as being on the lower surface 14 of the package 10 and attached to contact areas 9 on a representative carrier substrate 8. The dimensions of the package 10 include length 11, width 13 and ~~vertical~~ thickness 15 (exclusive of the distance outer connectors 18 protrude from the lower surface 14). The outline of the encapsulated package 10, comprising length 11 and width 13 dimensions, defines the "footprint" of the package 10. The package 10 shown in FIG. 1 represents a multidie package which has been encapsulated in a mold.

Please amend paragraph **[0060]** as follows:

[0060] In this discussion, the position of each semiconductor device relative to the interposer 61 will be noted as being at a ~~"first-level",~~ "first-level," i.e., within the receptacle 65, at a ~~"second-level,"~~ "second-level," i.e., above the upper surface 66 of the interposer 61, or at a ~~"third-level",~~ "third-level," i.e., below the lower surface 68 of the interposer 61. In addition, sublevels may exist within each level, each sublevel being occupied by a semiconductor device. Thus, a wide range of semiconductor device combinations may be achieved to meet a particular package's electronic footprint and thickness constraints for a particular purpose, whether that is for a microprocessor, memory device, or other purpose.

Please amend paragraph **[0065]** as follows:

[0065] In the embodiment of FIG. 2, interposer 61 includes contact areas 71A and 71B (e.g., contact pads) formed on the upper surface 66 thereof. Contact areas 71A are adjacent the receptacle 65 for wirebonding to bond pads 30 on the active surface(s) 22 of the first-level semiconductor device(s) 20. Each contact area 71B corresponds with and is configured to be electrically connected, via intermediate conductive elements 52, such as the depicted bond wires, conductive TAB elements carried by dielectric polymer film, thermocompression or ultrasonically bonded leads, or the like, to bond pads 50 on the active surface 42 of the ~~second-level~~ second-level semiconductor device 40. Thus, the contact areas 71B are located outside of the ~~second-level~~ second-level semiconductor device 40 to facilitate electrical connection to the intermediate conductive elements 52. The conductive elements 32, 52; bond pads 30, 50; contact areas 71A, 71B, 75; traces 72; and vias 78 may comprise, for example, aluminum, gold, silver, conductive alloys, or the like.

Please amend paragraph **[0071]** as follows:

[0071] Configuring second-level semiconductor device 40 to be mounted in a ~~flip-chip~~ flip-chip arrangement provides a package 110 with a reduced profile, inasmuch as intermediate conductive elements 52 are eliminated. Nevertheless, the package 110 is shown with encapsulant material 90 covering the second-level semiconductor device 40.

Please amend paragraph **[0072]** as follows:

[0072] The package 110′ of FIG. 4 differs from ~~the package~~ package 110 of FIG. 3 only in that the encapsulant material 90 is mold-applied to leave the back side 44 of the second-level semiconductor device 40 uncovered. For many applications, additional covering of the back side 44 is unnecessary; eliminating this encapsulant provides a further reduction in profile (package thickness 15 in FIG. 1).

Please amend paragraph **[0075]** as follows:

[0075] All of the packages discussed thus far include a first-level semiconductor device 20 which is electrically connected to an interposer by way of elongate intermediate conductive elements 32. In FIG. 7, an embodiment of package 110''' is depicted in which the first-level semiconductor device 20 is attached in flip-chip style to the back side 44 of the second-level semiconductor device 40 by way of solder balls 36 positioned between bond pads 30 of the first-level semiconductor device 20 and corresponding bond pads or other contact areas 59 on back side 44 of the second-level semiconductor device 40. Conductive traces 84 that are carried on the back side 44 of the second-level semiconductor device 40 extend from ~~bond pads~~ contact areas 59 toward an outer periphery of the second-level semiconductor device 40. Discrete conductive elements 82 electrically connect conductive traces 84 on the back side 44 of the second-level semiconductor device 40 to corresponding conductive traces 72 on the interposer 61. The second-level semiconductor device 40 is, in turn, electrically connected by elongate intermediate conductive elements 52 to contact areas 71B on the upper surface 66 of the interposer 61.

Please amend paragraph **[0077]** as follows:

[0077] In the package 210 of FIG. 8, bond pads 30 on the active surface 22 of a ~~first-level~~ first-level semiconductor device 20' are attached to contact areas 59 on the active surface 42 of a second-level semiconductor device 40 by discrete conductive elements 36A, shown comprising conductive balls, although bumps, pillars, columns, regions of films, and other structures formed from metal, conductive or conductor-filled elastomer, or the like (e.g., an anisotropic or ~~z-axis conductive~~ z-axis conductive film) could also be used. Conductive traces 54 on the active surface 42 of the second-level semiconductor device 40 connect the contact areas 59, via discrete conductive elements 56, traces 72, conductors 70 and conductive vias 78, to contact areas 75 and outer connectors 18. Bond pads 50 on the second-level semiconductor device 40 electrically communicate in a like manner with outer connectors 18. Although the first-level semiconductor device 20' in this example is shown with two centrally arranged rows of discrete conductive elements 36A, a semiconductor device 20' with peripherally

located discrete conductive elements 36A may be used with a second-level semiconductor device 40 that has shorter conductive traces 54 extending over the active surface 42 thereof.

Please amend paragraph **[0078]** as follows:

[0078] FIG. 9 depicts a package 210′ which varies from the embodiments already described. In the package 210′ of FIG. 9, a first-level semiconductor device 20 is not mounted within the interposer receptacle 65. Instead, a third-level semiconductor device 100 is mounted with an active surface 102 thereof facing upward toward the receptacle 65 and the lower surface 68 of the ~~interposer 61~~ interposer 161 and secured to the lower surface 68 with adhesive material 117. Bond pads 118 on the third-level semiconductor device 100 are shown connected to the active surface 42 of the second-level semiconductor device 40 by discrete conductive elements 116. The back side 104 of third-level semiconductor device 100 is shown uncovered, but may be encapsulated. In FIG. 9, the interposer ~~61~~ interposer 161 is shown as being formed from a flexible or so-called "flex" substrate material of a known type, which typically has a reduced thickness relative to rigid substrates.

Please amend paragraph **[0082]** as follows:

[0082] In FIG. 11, an embodiment of a package 310 is depicted in which two or more first-level semiconductor devices 20′ are positioned side-by-side within an interposer receptacle 65. The bond pads 30 of each semiconductor device 20′ are flip-chip bonded by discrete conductive elements 36 to corresponding contact areas 59 on the active surface 42 of a second-level semiconductor device 40. Like the embodiments of FIGS. 8, 9 and 10, the ~~second-level~~ second-level semiconductor device 40 is flip-chip bonded to the upper surface 66 of the interposer 61. FIG. 11 also illustrates an assembly structure 86, such as a film, which may be attached to the lower surface 68 of the interposer 61, covering the receptacle 65 before positioning and attaching the first-level semiconductor devices 20′ in the receptacle 65. This feature is useful in assembling packages where the first-level semiconductor devices 20′ are first mounted in the receptacle 65 of the interposer 61, followed by attachment of the second-level semiconductor device 40 to the interposer 61 and the first-level semiconductor devices 20′. The

assembly structure 86 may be temporarily or permanently attached to hold one or more first-level semiconductor devices 20′ in place prior to and while electronically connecting the same to the interposer 61. The assembly structure 86 may subsequently be removed.

Please amend paragraph **[0083]** as follows:

[0083] The embodiment of semiconductor device package 310′ shown in FIG. 12 includes a second-level semiconductor device 40 and a third-level semiconductor device 100 that are attached, flip-chip style, to the upper surface 66 and lower surface 68, respectively, of the interposer 61, as previously described. Within the interposer receptacle 65 are two first-level semiconductor devices 20A and 20B, one above the other. The upper first-level semiconductor device ~~20A'~~ 20A is attached flip-chip style to the active surface 42 of the second-level semiconductor device 40. The lower first-level semiconductor device 20B is attached, flip-chip style, to the active surface 102 of the third-level semiconductor device 100.

Please amend paragraph **[0087]** as follows:

[0087] FIGS. ~~13A-I~~ 13A-13I depict a method for assembling a multidie semiconductor device package such as that pictured in FIGS. 2, 2A, and 2B, for example. As shown in FIG. 13A, a plurality of first-level semiconductor devices 20 is prepared on an active surface 22 of a wafer 26 or other suitable semiconductor substrate, such as a substrate formed from gallium arsenide, indium phosphide, or another semiconductive material or a so-called silicon-on-insulator (SOI) type substrate (e.g., silicon-on-glass (SOG), silicon-on-ceramic (SOC), silicon-on-sapphire (SOS), etc.). Each semiconductor device 20 typically comprises semiconductor material with internal electronic functions and a plurality of bond pads (not shown) on the active surface 22. The wafer 26 is cut along saw lines 28, as depicted in FIG. 13B, to produce individual singulated first-level semiconductor devices 20.

Please amend paragraph **[0088]** as follows:

[0088] Likewise, as illustrated in FIG. 13C, a plurality of second-level semiconductor devices 40 is fabricated on an active surface 42 of a wafer 46 or other semiconductor substrate.

These second-level semiconductor devices 40 will generally be larger in footprint than the ~~first-level~~ first-level semiconductor devices 20. The wafer 46 is then cut along saw lines 48 into individual singulated second-level semiconductor devices 40, as shown in FIG. 13D.

Please amend paragraph **[0089]** as follows:

[0089] In addition, as depicted in FIG. 13E, a plurality of interposers 61 is formed from an interposer substrate material 60. The interposer substrate 60 may be in the form of a multi-interposer sheet or ~~strip 62,~~ strip, which is referred to herein as "sheet/strip 62," as represented in FIG. 13E, with an upper surface 66 and a lower surface 68. On one or both of the upper surface 66 and the lower surface 68 include metallization, including bond pads, contact areas, conductive traces, and/or the like, and conductive vias for vertical interconnection (not shown). Cut lines 64 are located between adjacent, individual interposers 61 of the sheet/strip 62 and form boundaries therebetween. Each interposer 61 includes a generally centrally positioned receptacle 65 formed at least partially therethrough, into which one or more first-level semiconductor devices 20 may be positioned and mounted. An assembly structure 86, such as film, may be temporarily or permanently attached to the lower surface 68 of each interposer 61 to cover the opening of the receptacle 65 thereof.

Please amend paragraph **[0090]** as follows:

[0090] Turning now to FIG. 13F, a first-level semiconductor device 20 may be placed in each receptacle 65. The first-level semiconductor device 20 may then be electrically connected to the interposer 61 by way of intermediate conductive elements 32. This may occur prior to separation of adjacent interposers 61 ~~from the~~ from sheet/strip 62, as shown, or following separation of the interposers 61 ~~from the~~ from sheet/strip 62.

Please amend paragraph **[0091]** as follows:

[0091] Next, as shown in FIG. 13G, individual second-level semiconductor devices 40 are positioned over each receptacle 65 containing a wire-bonded first-level semiconductor device 20. Each second-level semiconductor device 40 is attached to the upper surface 66 of the

interposer 61 by a dielectric adhesive material 58, such as ~~KAPTON™~~ KAPTON® tape, for example. Intermediate conductive elements 52 may then be positioned or formed between bond pads (not shown) of the second-level semiconductor device 40 and corresponding contact areas (not shown) of the interposer 61.

Please amend paragraph **[0093]** as follows:

[0093] For encapsulation of packages 10 in this invention, a suitable, known type of encapsulant material 90 (e.g., a filled polymer transfer molding compound or a silicone or ~~epoxy-type~~ epoxy-type glob-top type encapsulant material) is introduced into the remaining interstitial spaces 80 within receptacle 65 of each interposer 61 of the ~~substrate~~ sheet/strip 62. The encapsulant material 90 extends laterally between at least portions of the outer periphery of each first-level semiconductor device 20 within the receptacle 65 and the interstitial space 80 between the second-level semiconductor device 40 and the interposer 61. The encapsulant material 90 may also substantially cover the intermediate conductive elements including all bond pads, bond wires, intermediate connectors, contact areas, and traces. Accordingly, the encapsulant material 90 may substantially fill the remaining space within receptacle 65 and at least partially cover the active surface 22, 42, 102 of each semiconductor device 20, 40, 100 as well as the regions of the upper surface 66 of the interposer 61 at which metallization areas are located.

Please amend paragraph **[0095]** as follows:

[0095] As depicted in the figures, when encapsulant material 90 has hardened, set, or cured, the encapsulant material 90 holds the one or more first-level semiconductor devices 20 within the receptacle 65. Accordingly, an assembly structure or film 86 (FIG. 11) may be removed from the lower surface 68 of each interposer 61, with each first-level semiconductor device 20 being suspended in the receptacle 65 of that interposer 61 and the back side 24 of each first-level semiconductor device 20 within the receptacle 65 being exposed. An exemplary encapsulation of the assembly 86 with an encapsulant material 90 in a transfer mold or pot mold may be used to form interconnected packages 10 of uniform size, as illustrated, or separate packages 10 that include previously separated interposers 61.

Please amend paragraph **[0097]** as follows:

[0097] Another example of a method of the present invention, depicted in FIGS. ~~14A-I,~~ 14A-14I, is applicable to the packages shown in FIGS. 7, 8, 9, 10, 11, and 12, for example. A package formed by this method has the first-level semiconductor device 20 connected in a ~~flip-chip~~ flip-chip manner to a second-level semiconductor device 40.

Please amend paragraph **[00102]** as follows:

[00102] As shown in FIG. 14G, the two-die units 94 are attached to interposers 61 of ~~the multi-interposer substrate sheet or~~ sheet/strip 62 by flip-chip connection of the second-level semiconductor devices 40 to the interposers 61, with the first-level semiconductor devices 20 being received by receptacles 65 of the interposers 61. As shown, first-level semiconductor devices 20 project upwardly through the receptacles 65 of the inverted interposers 61. Each ~~first-level~~ first-level semiconductor device 20 and second-level semiconductor device 40 communicates with outer connectors 18 through the intermediate conductors (bond pads, contact areas, solder balls and vias, etc.).

Please amend paragraph **[00108]** as follows:

[00108] Continuing the assembly process, as shown in FIG. 15F, a plurality of ~~first-level~~ first-level semiconductor devices 20 is formed on an active surface 22 of wafer 26 or other semiconductor substrate, as previously described with reference to FIG. 13A. Discrete conductive elements 36 are attached to bond pads (not shown) on the active surfaces 22 of the first-level semiconductor devices 20. Next, as illustrated in FIG. 15G, the wafer 26 is cut along saw lines 28 to singulate first-level semiconductor devices 20 from one another.

Please amend paragraph **[00111]** as follows:

[00111] The encapsulated structure of FIG. 15I may be cut along cut lines 64 to form singulated packages 10. Alternatively, singulation may be effected prior to encapsulation. Each package 10 includes an upper surface 12 and a lower surface 14, which are identified in the respective upper and lower views of package 10 of FIGS. 15J and 15K. The packaging configuration is typical of that produced by known transfer molding or pot molding processes. Optionally, the encapsulation step may be configured to cover the exposed back sides of ~~second-level~~ second-level semiconductor device 40 and/or first-level semiconductor device 20. Optionally, any bare edges of the interposer, i.e., those exposed at cut lines 64, may be covered by an encapsulant in a subsequent step. The edges may be covered by an encapsulant, e.g., glob top, at the time that the package 10 is mounted on a carrier substrate.